REMARKS

Claims 1-20 remain pending in the instant application. Claims 1-20 presently stand rejected. Claims 1, 8, 11, and 13-15 are amended herein. Entry of this amendment and reconsideration of the pending claims are respectfully requested.

Drawings

The Examiner objected to the drawings under 37 CFR 1.83(a) stating, "in the method of claim 15, the step of dividing the data manipulation task and the instructions having a plurality of portions must be shown or the feature(s) canceled from the claim(s)." *Office Action* mailed December 12, 2003, page 2, section 3. However, Applicants respectfully point out that FIGs. 1 and 2 do indeed illustrate a "split instruction 20." A portion of the instruction is provided to the control engine 14 and other portions are provided to the coprocessors 18, as illustrated by the multi-head arrow labeled as "split instruction 20." This is described within the specification on page 7, lines 2-7. Accordingly, Applicants request that the Examiner withdraw the instant objection to the drawings.

Specification

The specification stands objected to "because it lacks a "BRIEF SUMMARY OF THE INVENTION section and the various sections appearing in the application should not be underlined.

Accordingly, Applicants have amended the specification to remove the underlining of the various sections.

Regarding the lack of a "Brief Summary of the Invention," Applicants would like to kindly point out that both the M.P.E.P. and 37 C.F.R. §1.73 do not require the presence of a "Summary of the Invention" in a patent application. Rather, they merely indicate where in the application the "Summary of the Invention" should be placed if Applicants were to elect to include one.

In particular, 37 C.F.R. §1.73 only states that "[a] brief summary of the invention ... should precede the detailed description." 37 C.F.R. § 1.73 does not state "must" or

"shall." Accordingly, Applicants have elected not to include a "Summary of the Invention" as this is within the discretion of the Applicants.

Claim Objections

Claims 1, 11, 13, and 14 stand objected to for a number of informalities. Accordingly, Applicants have amended claims 1, 11, 13, and 14 to address the Examiner's concerns.

Claim Rejections – 35 U.S.C. § 102

Claims 1-12 and 15-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,182,203 B1 to Simar, Jr. et al. (hereafter "Simar").

A claim is anticipated only if each and every element of the claim is found in a single reference. M.P.E.P § 2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628 (Fed. Cir. 1987)). "The identical invention must be shown in as complete detail as is contained in the claim." M.P.E.P. § 2131 (citing *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226 (Fed. Cir. 1989)).

Independent claim 1 recites, in pertinent part, "each of said control engine **and** plurality of coprocessors being enabled to perform simultaneous functions in response to a **single instruction**." Applicants respectfully submit that Simar fails to disclose a control engine and coprocessors to perform simultaneous functions in response to a single instruction.

The Examiner stated, "control registers 10a and the control logic 10b control the execution of instructions [col. 7 lines 5-6; col. 8 lines 37-43] and all of the functional units execute the instructions simultaneously in response to a single Very Long Instruction Word (VLIW) [col. 4 lines 64-67; col. 5 line 1; col. 33, lines 46-49])." Office Action mailed December 12, 2003, page 6, lines 11-15. However, col. 33, lines 46-49 of Simar in fact state,

> The very Long Instruction Word (VLIW) CPU of the present invention uses a 256-bit wide instruction to feed up to eight 32-bit instructions **to the eight functional units** during every clock cycle. (emphasis added)

Therefore, this portion of Simar simply discloses that functional units 12a1-12a4 and 12b1-12b4 receive portions of a 256-bit wide instruction. However, Simar fails to disclose **both** a control engine and coprocessors receiving portions of a single instruction to perform simultaneous functions in response to the single instruction.

To be sure, Simar discloses

> The program fetch 7a, instruction dispatch 7b, and instruction decode 7c units can **deliver** up to eight 32-bit **instructions** from the program memory 2 **to the functional units** every cycle.

Simar, col. 6, lines 64-67. Thus, Simar discloses that the elements, which the Examiner cites as corresponding to Applicants control engine (7a, 7b, and 7c), **deliver** instructions to the functional units, but does not disclose elements 7a, 7b, and 7c as performing **simultaneous** functions with the functional units. In fact, since fetch unit 7a, dispatch unit 7b, and decode unit 7c deliver instructions to the functional units, they cannot perform simultaneous functions with the functional units based on a single instruction. Rather, the functional units 12a1-12a4 and 12b1-12b4 can only perform functions until **after** fetch unit 7a, dispatch unit 7b, and decode unit 7c **deliver** the 32-bit instructions. In short, fetch 7a, dispatch 7b, and decode 7c are earlier in the data path (see FIG. 1 of Simar) and therefore do not perform **simultaneous** functions with the functional units, in response to a **single instruction**.

Consequently, Simar fails to disclose each and every element of claim 1, as required under M.P.E.P. § 2131. Accordingly, Applicants request that the instant §102 rejection be withdrawn.

Amended independent claim 8, now recites in pertinent part, "wherein the data memory, the microcontroller, the instruction memory, and the first and second coprocessors are **coupled in parallel**." Similarly, amended independent claim 15 now recites, in pertinent part, "a processing machine including a control engine and a plurality of coprocessors **coupled in parallel**...."

However, FIG. 1 of Simar illustrates program fetch 7a, instruction dispatch 7b, and instruction decode 7c (elements cited by the Examiner as corresponding to Applicants' claimed microcontroller) as **coupled in series** with functional units 12a1-12a4 and 12b1-12b4.

Consequently, Simar fails to disclose each and every element of claims 8 and 15, as required under M.P.E.P. § 2131. Accordingly, Applicants request that the instant §102 rejections of claims 8 and 15 be withdrawn.

Claim Rejections – 35 U.S.C. § 103

Claims 13 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Simar in view of U.S. Patent No. 5,548,587 to Bailey et al. (hereafter "Bailey").

Dependent claims 2-7, 9-14, and 16-20 are patentable over the prior art of record for at least the same reasons as discussed above in connection with their respective independent claims, in addition to adding further limitations of their own. Accordingly, Applicants respectfully request that the instant §§ 102 and 103 rejections for claims 2-7, 9-14, and 16-20 be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants believe the applicable rejections have been overcome and all claims remaining in the application are presently in condition for allowance. Accordingly, favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

CHARGE DEPOSIT ACCOUNT

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a). Any fees required therefore are hereby authorized to be charged to Deposit Account No. 02-2666. Please credit any overpayment to the same deposit account.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: Feb. 9, 2004

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FIRST CLASS CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

on February 9, 2004
Date of Deposit

Adrian Villarreal

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Date